ABSTRACT OF THE DISCLOSURE

For writing K-bit write data in parallel (K is integer at least 2), bit lines each arranged for each memory cell columns and at least K current return lines are provided. K selected bit lines to write the K-bit write data are connected in series in a single current path. When data having different levels are written through adjacent selected bit lines, the selected bit lines are connected to each other at their one ends or the other ends, so that a bit line write current flowing through the former selected bit line is directly transmitted to the latter selected bit line. On the other hand, when data having the same level are written through adjacent selected bit lines, a bit line write current flowing through the former selected bit line is turned back by the corresponding current return line, and then transmitted to the latter selected bit line.